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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,714	07/15/2003	David J. Corisis	108298532US1	9586

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PERKINS COIE LLP
PATENT-SEA
P.O. BOX 1247
SEATTLE, WA 98111-1247

EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 09/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/620,714	CORISIS	
	Examiner	Art Unit	
	Alexander O Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *50-77* is/are pending in the application.

4a) Of the above claim(s) *56,75 and 78-83* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *50-55,57-74,76 and 77* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/17/03 & 6/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/620714 Attorney's Docket #: 108298532US1
Filing Date: 7/15/2003;

Applicant: Corisis

Examiner: Alexander Williams

Applicant's election of species of figure 3 (claims 50-55, 57-74, 76 and 77), filed 6/29/04, has been acknowledged.

Applicant's Pre-Amendment filed 7/15/03 has been acknowledged.

This application contains claims 56, 75 and 78-83 drawn to an invention non-elected without traverse in Paper No. 4.

Claims 1-49 have been canceled.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The disclosure is objected to because of the following informalities: The divisional application information should be updated with the patent information.

Appropriate correction is required.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Initially, it is noted that the 35 U.S.C. § 103 rejection based on a first encapsulant and a second encapsulant deals with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a multi-piece structure into a one-piece structure. Generally, favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure.

Claims 50, 51, 53, 55, 57-59, 62-64, 67-69, 72, 73 and 77 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ball (U.S. Patent # 6,784,023 B2).
50. Ball (figures 1 to 9) specifically figure 6 show a packaged microelectronic devices **600**, comprising: a support member **606** having support member circuitry; a first packaged microelectronic device **604** connected to at least one of the support member and the support member circuitry and having a first microelectronic die at least partially encased **(by 634)** in a first encapsulant **634** to define a first package configuration; and a second packaged microelectronic device **602** connected to at least one of the support member and the support member circuitry with the first packaged microelectronic device

positioned between the support member and the second packaged microelectronic device, the second packaged microelectronic device having a second microelectronic die at least partially encased **(by 634)** in a second encapsulant **634** to define a second package configuration different than the first package configuration.

51. The assembly of claim 50, Ball further comprising a conductive connecting member **628** connected directly between the second packaged microelectronic device and the support member circuitry, at least a portion of the connecting member being positioned adjacent to an outer edge of the first packaged microelectronic device.

53. The assembly of claim 50, Ball show wherein the first packaged microelectronic device has a first planform shape in a plane generally parallel to a plane of the support member and the second packaged microelectronic device has a second planform shape in a plane generally parallel to the plane of the support member, and further wherein the second planform shape is more extensive in at least one direction generally parallel to the plane of the support member than is the first planform shape.

55. The assembly of claim 50, Ball show wherein the second packaged microelectronic device has a plurality of conductive members **628** electrically coupled to the second microelectronic die and extending away from the second encapsulant, further wherein all the conductive members extending away from the second encapsulant are attached directly between the second packaged microelectronic device and the support member circuitry without being attached to the first packaged microelectronic device.

57. Ball (figures 1 to 9) specifically figure 6 show an assembly of packaged microelectronic devices, comprising: a support member **606**; a first packaged microelectronic device **604** connected to the support member and having a first microelectronic die at least partially encased in a first encapsulant **634** to define a first planform shape; and a second packaged microelectronic device **602** connected to the support member with the first packaged microelectronic device positioned between the support member and the second packaged microelectronic device, the second packaged microelectronic device having a second microelectronic die at least partially encased in a second encapsulant **634** to define a second planform shape different than the first planform shape.

58. The assembly of claim 57, Ball show wherein the support member **606** defines a support member plane and the first planform shape describes an area in a first plane generally parallel to the support member plane that is smaller than an area described by

the second planform shape in a second plane generally parallel to the support member plane.

59. The assembly of claim 57, Ball further comprising a conductive connecting member **628** connected directly between the second packaged microelectronic device and the support member circuitry, at least a portion of the connecting member being positioned adjacent to the first packaged microelectronic device.

62. The assembly of claim 57, Ball show wherein the second packaged microelectronic device has a plurality of conductive members **628** electrically coupled to the microelectronic substrate and extending away from the second encapsulant, further wherein all the conductive members extending away from the second encapsulant are attached directly between the second packaged microelectronic device and the support member circuitry.

63. Ball (figures 1 to 9) specifically figure 6 show an assembly of packaged microelectronic devices, comprising: a support member **606**; a first packaged microelectronic device **604** having a first microelectronic die at least partially encased in a first encapsulant **634** and connected to the support member with a plurality of solder balls **610**; and a second packaged microelectronic device **602** having a second microelectronic die at least partially encased in a second encapsulant **634** and connected to the support member with a plurality of elongated connection members **628** extending from the second packaged microelectronic device around at least part of the first packaged microelectronic device and attached directly to the support member.

64. The assembly of claim 63, Ball show wherein the first packaged microelectronic device includes a first surface facing toward the support member, a second surface facing away from the support member and toward the second packaged microelectronic device, and a plurality of third surfaces between the first and second surfaces, further wherein the elongated connection members **628** are positioned adjacent to the third surfaces of the first packaged microelectronic device.

67. The assembly of claim 63, Ball show wherein the support member includes support member circuitry, and further wherein all the elongated connection members **628** of the second microelectronic device are attached directly to the support member circuitry.

68. Ball (figures 1 to 9) specifically figure 6 show an assembly of packaged microelectronic devices, comprising: a support member **606** having support member circuitry; a first packaged microelectronic device **604** electrically coupled directly to the support member circuitry; and a second packaged microelectronic device **602**

electrically coupled directly to the support member circuitry without any direct electrical connections **628** to the first packaged microelectronic device, the first packaged microelectronic device being positioned between the support member and the second packaged microelectronic device.

69. The assembly of claim 68, Ball further comprising an elongated conductive connecting member **628** connected between the second packaged microelectronic device and the support member circuitry, at least a portion of the connecting member being positioned adjacent to the first packaged microelectronic device.

72. The assembly of claim 68, Ball show wherein the first packaged microelectronic device is electrically coupled to the second packaged microelectronic device via the support member circuitry.

73. Ball (figures 1 to 9) specifically figure 6 show an assembly of packaged microelectronic devices, comprising: a support member **606** having support member circuitry; a first packaged microelectronic device **604** electrically coupled directly to the support member circuitry; and a second packaged microelectronic device **602** connected directly to the support member with the first packaged microelectronic device being positioned between the support member and the second packaged microelectronic device, the second packaged microelectronic device not being fixedly attached to the first packaged microelectronic device.

77. The assembly of claim 73, Ball show wherein the second packaged microelectronic device has a plurality of conductive members electrically coupled to the microelectronic substrate and extending away from an encapsulant of the second microelectronic device, further wherein all the conductive members extending away from an encapsulant of the second microelectronic device are attached directly between the second packaged microelectronic device and the support member circuitry.

Therefore, it would have been obvious to one of ordinary skill in the art to use the first and second encapsulants the as "merely a matter of obvious engineering choice" as set forth in the above case law.

Claims 50-55, 57-62, 68, 70 to 74, 76 and 77 are rejected under 35 U.S.C. § 102(b) as being anticipated by Venkateshwaran et al. (U.S. Patent # 6,339,254 B1).

50. Venkateshwaran et al. (figures 4 to 7) specifically figure 6A show an assembly of packaged microelectronic devices, comprising: a support member **610** having support

member circuitry; a first packaged microelectronic device **402** connected to at least one of the support member and the support member circuitry and having a first microelectronic die at least partially encased in a first encapsulant **410** to define a first package configuration; and a second packaged microelectronic device **401** connected to at least one of the support member and the support member circuitry with the first packaged microelectronic device positioned between the support member and the second packaged microelectronic device, the second packaged microelectronic device having a second microelectronic die at least partially encased in a second encapsulant to define a second package configuration different than the first package configuration.

51. The assembly of claim 50, Venkateshwaran et al. further comprising a conductive connecting member **411** connected directly between the second packaged microelectronic device and the support member circuitry, at least a portion of the connecting member being positioned adjacent to an outer edge of the first packaged microelectronic device.

52. The assembly of claim 50, Venkateshwaran et al. show wherein the first packaged microelectronic device has a first edge and a second edge facing opposite the first edge and the second packaged microelectronic device has a third edge and a fourth edge facing opposite the third edge, and wherein the third edge of the second packaged microelectronic device extends outwardly beyond the first edge of the first packaged microelectronic device and the fourth edge of the second packaged microelectronic device extends outwardly beyond the second edge of the first packaged microelectronic device.

53. The assembly of claim 50, Venkateshwaran et al. show wherein the first packaged microelectronic device has a first planform shape in a plane generally parallel to a plane of the support member and the second packaged microelectronic device has a second planform shape in a plane generally parallel to the plane of the support member, and further wherein the second planform shape is more extensive in at least one direction generally parallel to the plane of the support member than is the first planform shape.

54. The assembly of claim 50, Venkateshwaran et al. show wherein the second packaged microelectronic device is spaced apart from the first packaged microelectronic device to define a gap between the packaged devices.

55. The assembly of claim 50, Venkateshwaran et al. show wherein the second packaged microelectronic device has a plurality of conductive members **411** electrically coupled to the second microelectronic die and extending away from the second

encapsulant, further wherein all the conductive members extending away from the second encapsulant are attached directly between the second packaged microelectronic device and the support member circuitry without being attached to the first packaged microelectronic device.

57. Venkateshwaran et al. (figures 4 to 7) specifically figure 6A show an assembly of packaged microelectronic devices, comprising: a support member **610**; a first packaged microelectronic device **402** connected to the support member and having a first microelectronic die at least partially encased in a first encapsulant **410** to define a first planform shape; and a second packaged microelectronic device **401** connected to the support member with the first packaged microelectronic device positioned between the support member and the second packaged microelectronic device, the second packaged microelectronic device having a second microelectronic die at least partially encased in a second encapsulant to define a second planform shape different than the first planform shape.

58. The assembly of claim 57, Venkateshwaran et al. show wherein the support member defines a support member plane and the first planform shape describes an area in a first plane generally parallel to the support member plane that is smaller than an area described by the second planform shape in a second plane generally parallel to the support member plane.

59. The assembly of claim 57, Venkateshwaran et al. further comprising a conductive connecting member **411** connected directly between the second packaged microelectronic device and the support member circuitry, at least a portion of the connecting member being positioned adjacent to the first packaged microelectronic device.

60. The assembly of claim 57, Venkateshwaran et al. show wherein the first packaged microelectronic device has a first edge and a second edge facing opposite the first edge and the second packaged microelectronic device has a third edge and a fourth edge facing opposite the third edge, and wherein the third edge of the second packaged microelectronic device extends outwardly beyond the first edge of the first packaged microelectronic device and the fourth edge of the second packaged microelectronic device extends outwardly beyond the second edge of the first packaged microelectronic device.

61. The assembly of claim 57, Venkateshwaran et al. show wherein the second packaged microelectronic device is spaced apart from the first packaged microelectronic device to define a gap between the packaged devices.
62. The assembly of claim 57, Venkateshwaran et al. show wherein the second packaged microelectronic device has a plurality of conductive members **411** electrically coupled to the microelectronic substrate and extending away from the second encapsulant, further wherein all the conductive members extending away from the second encapsulant are attached directly between the second packaged microelectronic device and the support member circuitry.
68. Venkateshwaran et al. (figures 4 to 7) specifically figure 6A an assembly of packaged microelectronic devices, comprising: a support member **610** having support member circuitry; a first packaged microelectronic device **402** electrically coupled directly to the support member circuitry; and a second packaged microelectronic device 401 electrically coupled directly to the support member circuitry without any direct electrical connections to the first packaged microelectronic device, the first packaged microelectronic device being positioned between the support member and the second packaged microelectronic device.
70. The assembly of claim 68, Venkateshwaran et al. show wherein the first packaged microelectronic device has a first edge and a second edge facing opposite the first edge and the second packaged microelectronic device has a third edge and a fourth edge facing opposite the third edge, and wherein the third edge of the second packaged microelectronic device extends outwardly beyond the first edge of the first packaged microelectronic device and the fourth edge of the second packaged microelectronic device extends outwardly beyond the second edge of the first packaged microelectronic device.
71. The assembly of claim 68, Venkateshwaran et al. show wherein the second packaged microelectronic device is spaced apart from the first packaged microelectronic device to define a gap between the packaged devices.
72. The assembly of claim 68, Venkateshwaran et al. show wherein the first packaged microelectronic device is electrically coupled to the second packaged microelectronic device via the support member circuitry.
73. Venkateshwaran et al. (figures 4 to 7) specifically figure 6A show an assembly of packaged microelectronic devices, comprising: a support member **610** having support member circuitry; a first packaged microelectronic device **402** electrically coupled

directly to the support member circuitry; and a second packaged microelectronic device **401** connected directly to the support member with the first packaged microelectronic device being positioned between the support member and the second packaged microelectronic device, the second packaged microelectronic device not being fixedly attached to the first packaged microelectronic device.

74. The assembly of claim 73, Venkateshwaran et al. show wherein the second packaged microelectronic device is spaced apart from the first packaged microelectronic device to define a gap between the first and second packaged microelectronic devices.

76. The assembly of claim 73, Venkateshwaran et al. show wherein the first packaged microelectronic device has a first edge and a second edge facing opposite the first edge and the second packaged microelectronic device has a third edge and a fourth edge facing opposite the third edge, and wherein the third edge of the second packaged microelectronic device extends outwardly beyond the first edge of the first packaged microelectronic device and the fourth edge of the second packaged microelectronic device extends outwardly beyond the second' edge of the first packaged microelectronic device.

77. The assembly of claim 73, Venkateshwaran et al. show wherein the second packaged microelectronic device has a plurality of conductive members **411** electrically coupled to the microelectronic substrate and extending away from an encapsulant of the second microelectronic device, further wherein all the conductive members extending away from an encapsulant of the second microelectronic device are attached directly between the second packaged microelectronic device and the support member circuitry.

Therefore, it would have been obvious to one of ordinary skill in the art to use the first and second encapsulants the as "merely a matter of obvious engineering choice" as set forth in the above case law.

Claims 50-53, 55, 57-60, 62-70, 72, 73, 76 and 77 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Tamaki et al. (U.S. Patent # 6,157,080).

50. Tamaki et al. (figures 1 to 15) specifically figure 15 show a packaged microelectronic devices, comprising: a support member **21** having support member circuitry; a first packaged microelectronic device **1** connected to at least one of the support member and the support member circuitry and having a first microelectronic die

at least partially encased **(by 20)** in a first encapsulant **20** to define a first package configuration; and a second packaged microelectronic device **2** connected to at least one of the support member and the support member circuitry with the first packaged microelectronic device positioned between the support member and the second packaged microelectronic device, the second packaged microelectronic device having a second microelectronic die at least partially encased **(by 20)** in a second encapsulant to define a second package configuration different than the first package configuration.
51. The assembly of claim 50, Tamaki et al. further comprising a conductive connecting member **8** connected directly between the second packaged microelectronic device and the support member circuitry, at least a portion of the connecting member being positioned adjacent to an outer edge of the first packaged microelectronic device.
52. The assembly of claim 50, Tamaki et al. show wherein the first packaged microelectronic device has a first edge and a second edge facing opposite the first edge and the second packaged microelectronic device has a third edge and a fourth edge facing opposite the third edge, and wherein the third edge of the second packaged microelectronic device extends outwardly beyond the first edge of the first packaged microelectronic device and the fourth edge of the second packaged microelectronic device extends outwardly beyond the second*edge of the first packaged microelectronic device.
53. The assembly of claim 50, Tamaki et al. show wherein the first packaged microelectronic device has a first planform shape in a plane generally parallel to a plane of the support member and the second packaged microelectronic device has a second planform shape in a plane generally parallel to the plane of the support member, and further wherein the second planform shape is more extensive in at least one direction generally parallel to the plane of the support member than is the first planform shape.
55. The assembly of claim 50, Tamaki et al. show wherein the second packaged microelectronic device has a plurality of conductive members electrically coupled to the second microelectronic die and extending away from the second encapsulant, further wherein all the conductive members extending away from the second encapsulant are attached directly between the second packaged microelectronic device and the support member circuitry without being attached to the first packaged microelectronic device.
57. Tamaki et al. (figures 1 to 15) specifically figure 15 show an assembly of packaged microelectronic devices, comprising: a support member **21**; a first packaged microelectronic device **1** connected to the support member and having a first

microelectronic die at least partially encased **(by 20)** in a first encapsulant **20** to define a first planform shape; and a second packaged microelectronic device **2** connected to the support member with the first packaged microelectronic device positioned between the support member and the second packaged microelectronic device, the second packaged microelectronic device having a second microelectronic die at least partially encased **(by 20)** in a second encapsulant **20** to define a second planform shape different than the first planform shape.

58. The assembly of claim 57, Tamaki et al. show wherein the support member defines a support member plane and the first planform shape describes an area in a first plane generally parallel to the support member plane that is smaller than an area described by the second planform shape in a second plane generally parallel to the support member plane.

59. The assembly of claim 57, Tamaki et al. further comprising a conductive connecting member **8** connected directly between the second packaged microelectronic device and the support member circuitry, at least a portion of the connecting member being positioned adjacent to the first packaged microelectronic device.

60. The assembly of claim 57, Tamaki et al. show wherein the first packaged microelectronic device has a first edge and a second edge facing opposite the first edge and the second packaged microelectronic device has a third edge and a fourth edge facing opposite the third edge, and wherein the third edge of the second packaged microelectronic device extends outwardly beyond the first edge of the first packaged microelectronic device and the fourth edge of the second packaged microelectronic device extends outwardly beyond the second edge of the first packaged microelectronic device.

62. The assembly of claim 57, Tamaki et al. show wherein the second packaged microelectronic device has a plurality of conductive members **8** electrically coupled to the microelectronic substrate and extending away from the second encapsulant, further wherein all the conductive members **8** extending away from the second encapsulant are attached directly between the second packaged microelectronic device and the support member circuitry.

63. Tamaki et al. (figures 1 to 15) specifically figure 15 show an assembly of packaged microelectronic devices, comprising: a support member **21**; a first packaged microelectronic device **1** having a first microelectronic die at least partially encased **(by 20)** in a first encapsulant **20** and connected to the support member with a plurality of

solder balls **22**; and a second packaged microelectronic device 2 having a second microelectronic die at least partially encased **(by 20)** in a second encapsulant **20** and connected to the support member with a plurality of elongated connection members **8** extending from the second packaged microelectronic device around at least part of the first packaged microelectronic device and attached directly to the support member.

64. The assembly of claim 63, Tamaki et al. show wherein the first packaged microelectronic device includes a first surface facing toward the support member, a second surface facing away from the support member and toward the second packaged microelectronic device, and a plurality of third surfaces between the first and second surfaces, further wherein the elongated connection members are positioned adjacent to the third surfaces of the first packaged microelectronic device.

65. The assembly of claim 63, Tamaki et al. show wherein the first packaged microelectronic device has a first edge and a second edge facing opposite the first edge and the second packaged microelectronic device has a third edge and a fourth edge facing opposite the third edge, and wherein the third edge of the second packaged microelectronic device extends outwardly beyond the first edge of the first packaged microelectronic device and the fourth edge of the second packaged microelectronic device extends outwardly beyond the second edge of the first packaged microelectronic device.

66. The assembly of claim 63, Tamaki et al. show wherein the second packaged microelectronic device is spaced apart **(by 15)** from the first packaged microelectronic device to define a gap **(portion where 15 sits)** between the packaged devices.

67. The assembly of claim 63, Tamaki et al. show wherein the support member includes support member circuitry, and further wherein all the elongated connection members **8** of the second microelectronic device are attached directly to the support member circuitry.

68. Tamaki et al. (figures 1 to 15) specifically figure 15 show an assembly of packaged microelectronic devices, comprising: a support member **21** having support member circuitry; a first packaged microelectronic device **1** electrically coupled directly to the support member circuitry; and a second packaged microelectronic device **2** electrically coupled directly to the support member circuitry without any direct electrical connections to the first packaged microelectronic device, the first packaged microelectronic device being positioned between the support member and the second packaged microelectronic device.

69. The assembly of claim 68, Tamaki et al. show further comprising an elongated conductive connecting member **8** connected between the second packaged microelectronic device and the support member circuitry, at least a portion of the connecting member being positioned adjacent to the first packaged microelectronic device.

70. The assembly of claim 68, Tamaki et al. show wherein the first packaged microelectronic device has a first edge and a second edge facing opposite the first edge and the second packaged microelectronic device has a third edge and a fourth edge facing opposite the third edge, and wherein the third edge of the second packaged microelectronic device extends outwardly beyond the first edge of the first packaged microelectronic device and the fourth edge of the second packaged microelectronic device extends outwardly beyond the second edge of the first packaged microelectronic device.

72. The assembly of claim 68 wherein the first packaged microelectronic device is electrically coupled to the second packaged microelectronic device via the support member circuitry.

73. Tamaki et al. (figures 1 to 15) specifically figure 15 show an assembly of packaged microelectronic devices, comprising: a support member **21** having support member circuitry; a first packaged microelectronic device **1** electrically coupled directly to the support member circuitry; and a second packaged microelectronic device **2** connected directly to the support member with the first packaged microelectronic device being positioned between the support member and the second packaged microelectronic device, the second packaged microelectronic device not being fixedly attached to the first packaged microelectronic device.

76. The assembly of claim 73, Tamaki et al. show wherein the first packaged microelectronic device has a first edge and a second edge facing opposite the first edge and the second packaged microelectronic device has a third edge and a fourth edge facing opposite the third edge, and wherein the third edge of the second packaged microelectronic device extends outwardly beyond the first edge of the first packaged microelectronic device and the fourth edge of the second packaged microelectronic device extends outwardly beyond the second' edge of the first packaged microelectronic device.

77. The assembly of claim 73, Tamaki et al. show wherein the second packaged microelectronic device has a plurality of conductive members **8** electrically coupled to

the microelectronic substrate and extending away from an encapsulant of the second microelectronic device, further wherein all the conductive members **8** extending away from an encapsulant of the second microelectronic device are attached directly between the second packaged microelectronic device and the support member circuitry.

Therefore, it would have been obvious to one of ordinary skill in the art to use the first and second encapsulants the as "merely a matter of obvious engineering choice" as set forth in the above case law.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/686,685,777,723,737,734,738,778,779,772,666,673, 668,687,678	8/31/04
Other Documentation: foreign patents and literature in 257/686,685,777,723,737,734,738,778,779,772,666,673, 668,687,678	8/31/04
Electronic data base(s): U.S. Patents EAST	8/31/04

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW
8/31/04

Primary Patent Examiner
Alexander O. Williams